URN etd-0407109-183726-2193
Author Yun Hsiun Hung
Author's Email Address No Public.
Statistics This thesis had been viewed 71 times. Download 40 times.
Department
Year 2006
Semester 2
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title A 16 Bit Adder/Subtractor Using Hybrid IGDI/CMOS Design
Date of Defense 0000-00-00
Page Count 52

Keyword
IGDI
FA

Abstract
GDI (Gate Diffusion Input) is a new technique which was proposed in few years ago. This technique allows reducing power consumption, delay time and area of circuit. The most important feature of the GDI circuit is to simplify the design of a complicated digital circuit. Although there are many different circuits that can be used to improve speed, reduce power consumption and area of circuit, most of these circuits are very complex. Among these circuits, PTL (Pass-Transistor Logic) is one of the most common low power circuits. However, it is very difficult and complex to design a PTL circuit from top to down. Since there is no suitable and simple cell library for designers to use. Adder is one of the most common operation units in ALU (Arithmetic Logic Unit), e.g, subtractor, multiplier, and divider, which are all based on the adder.
This thesis is based on the GDI circuit which is used to propose a brand new 16 bit IGDI adder/subtractor. We have compared the power consumption, speed, and number of transistors with other adders. We can find that the adder /subtractor based on the IGDI structure has less power consumption and high speed.
Advisory Committee Po Ming Lee - advisor

Files etd-0407109-183726-2193-001.pdf

indicate access worldwide
Date of Submission 2007-07-17